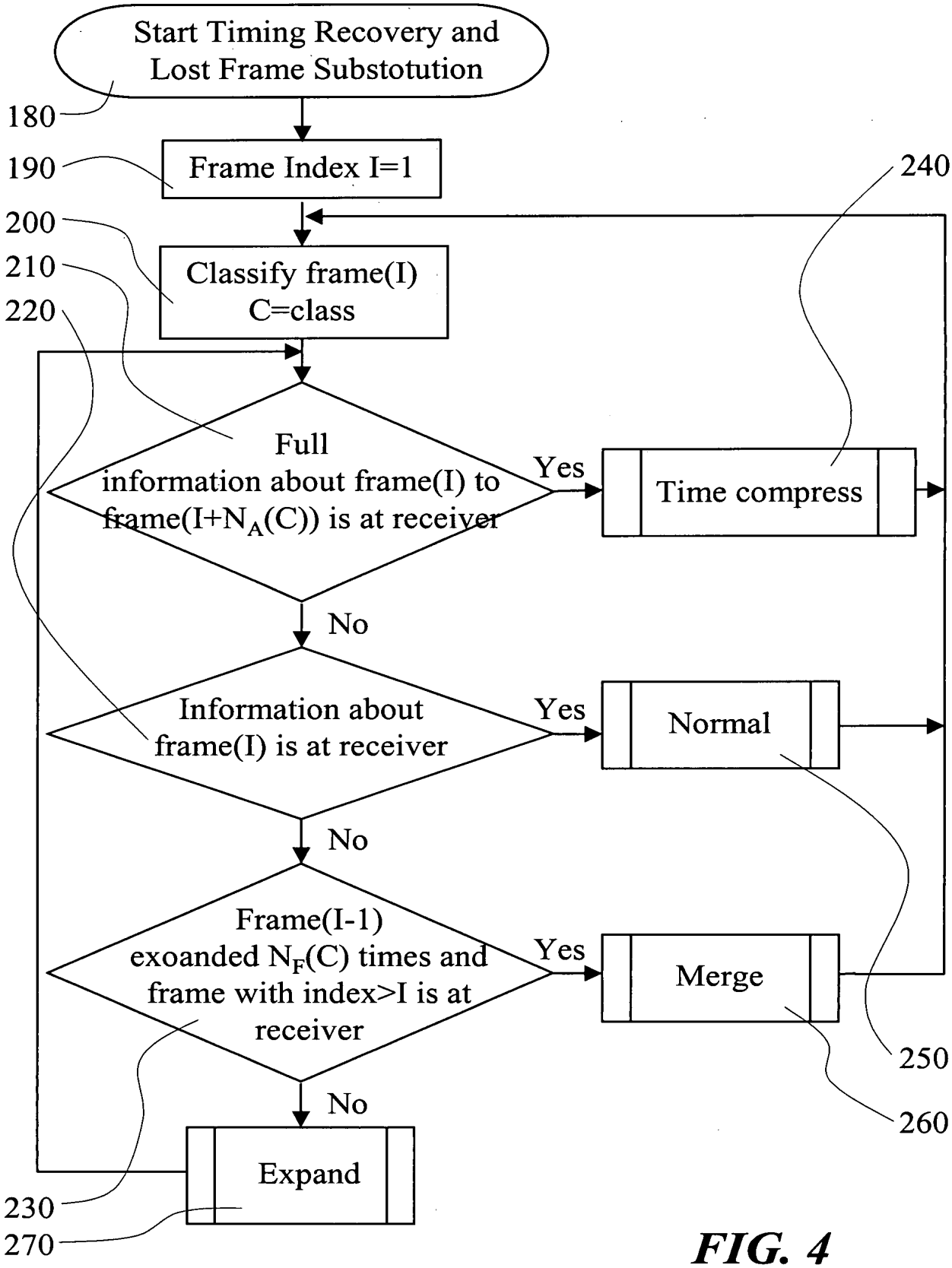

FIG. 4

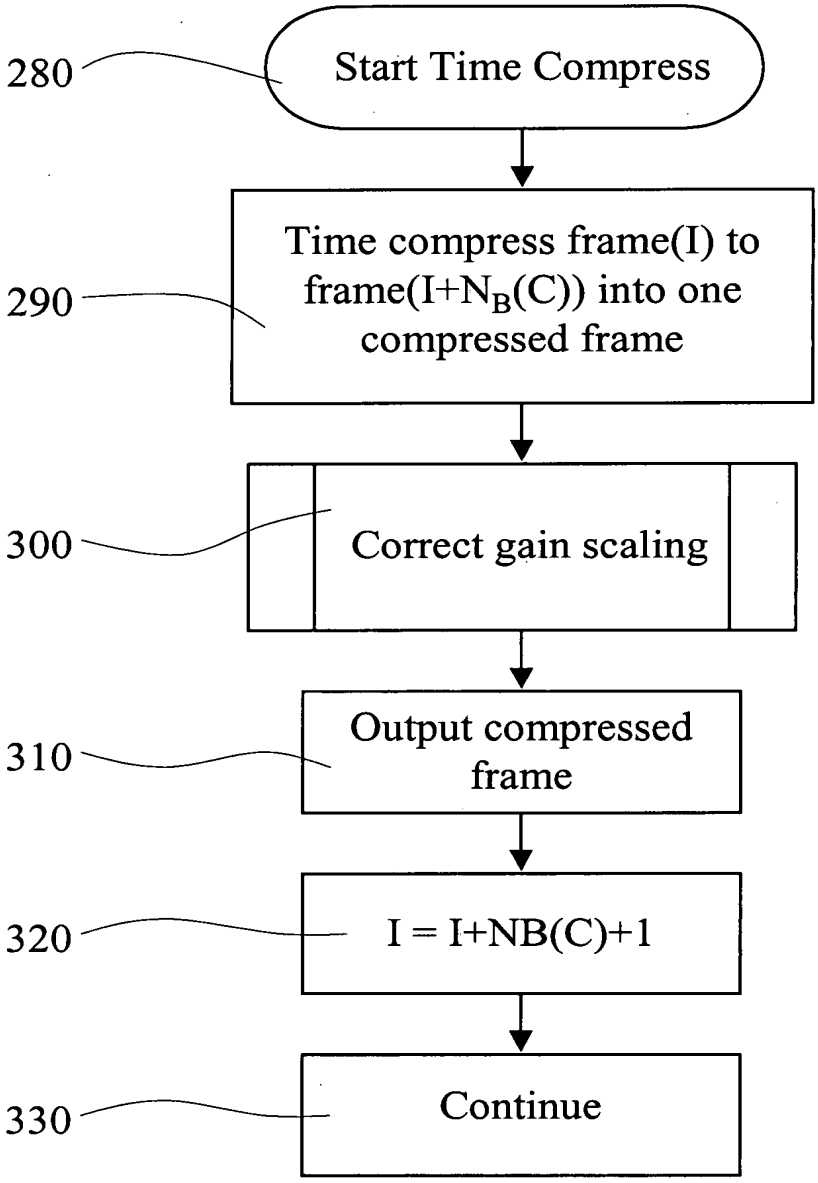

FIG. 5

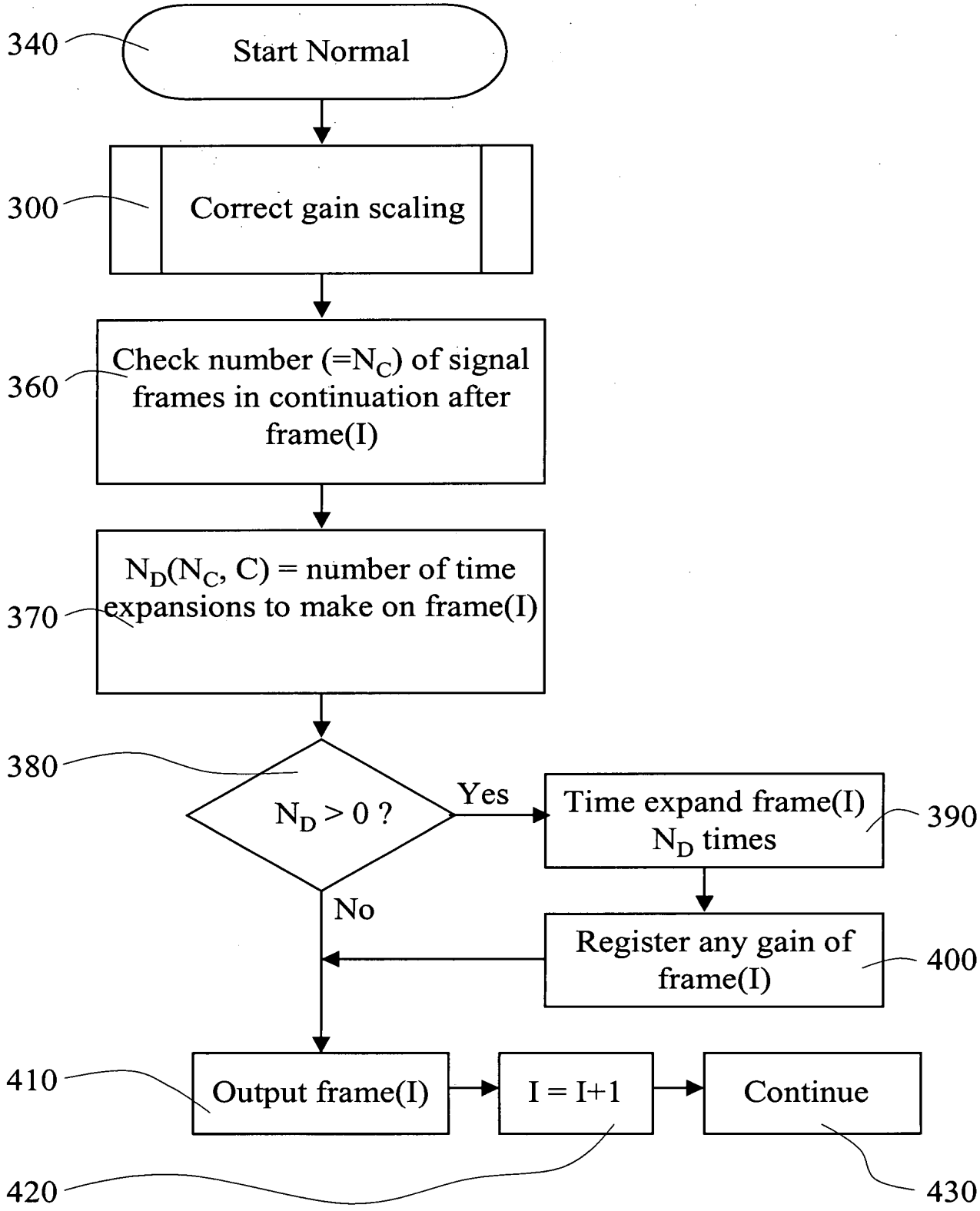

FIG. 6

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FIG. 10a

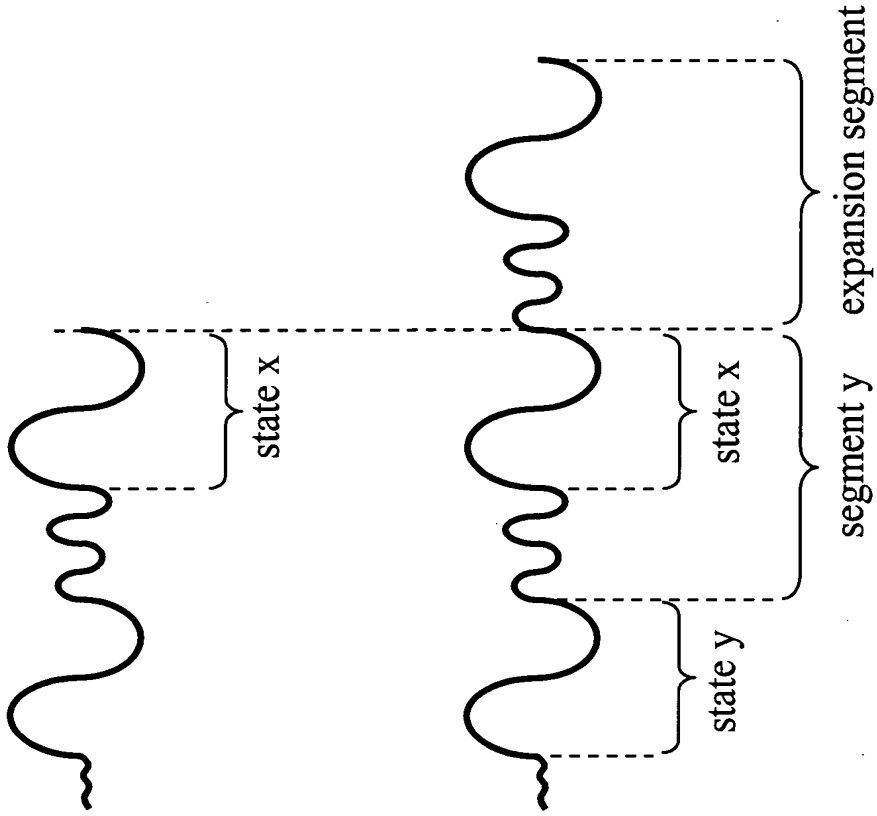
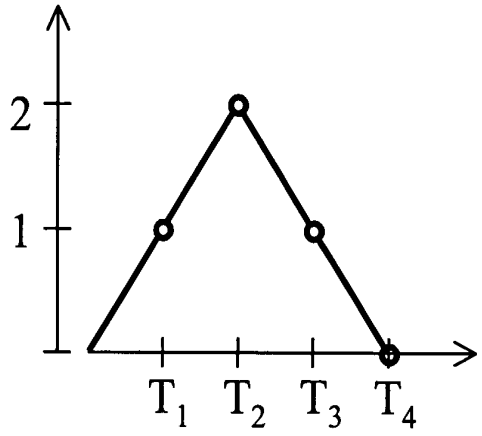
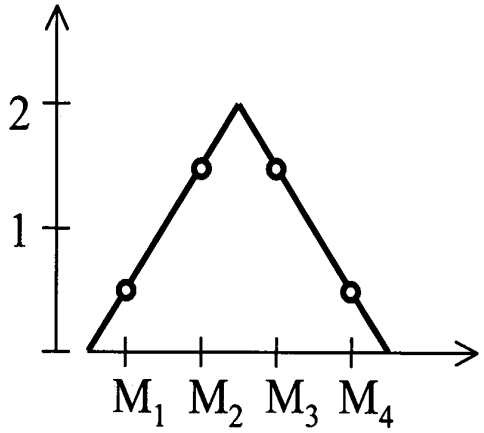


FIG. 10b



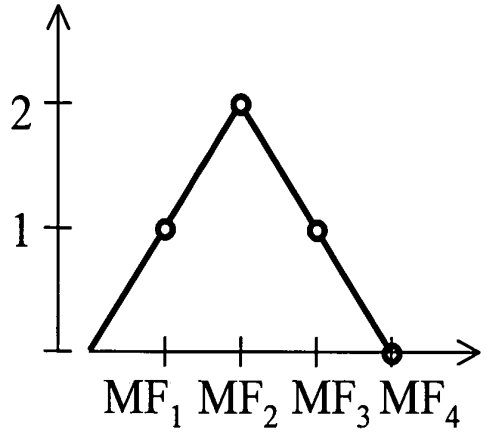
True state

FIG. 11a



State with no fractional delay

FIG. 11b



State with fractional delay 1/2

FIG. 11c

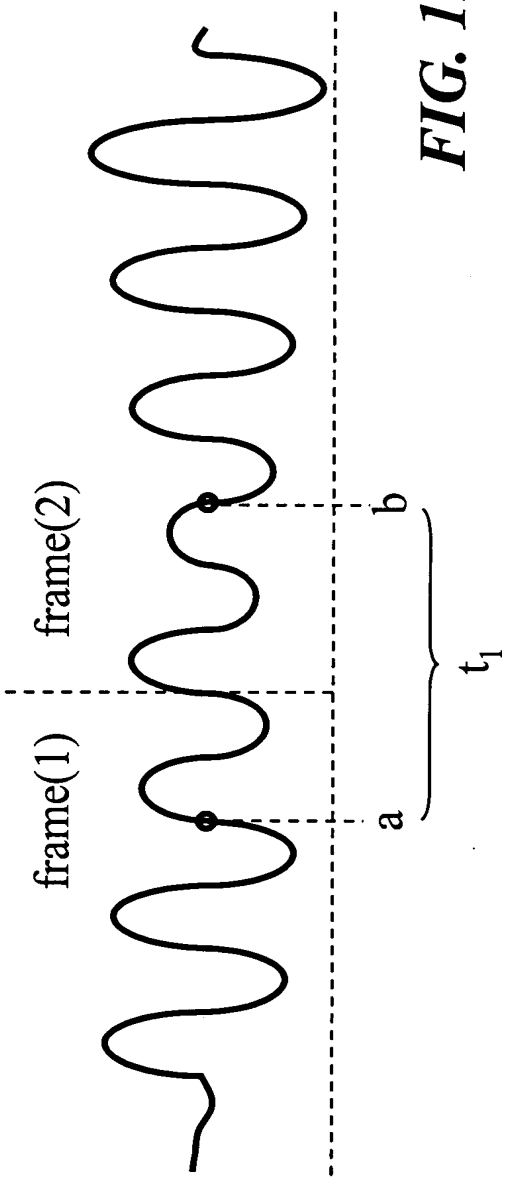


FIG. 12a

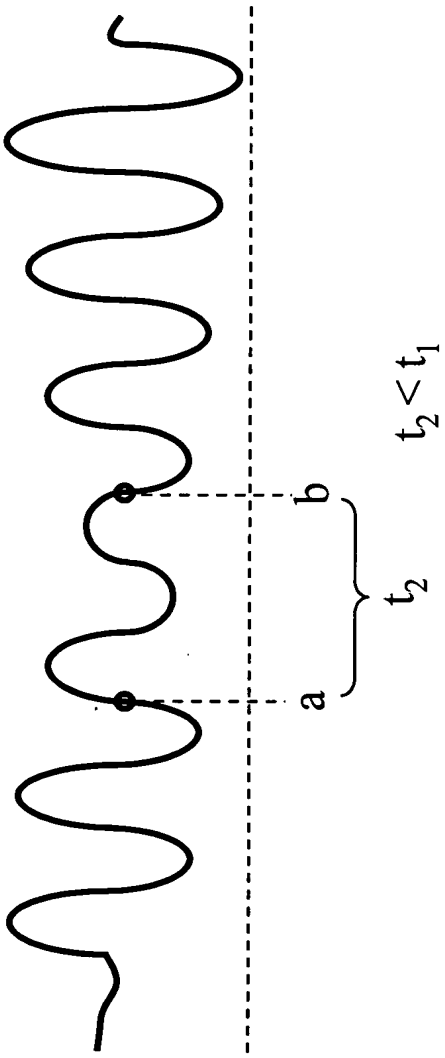


FIG. 12b